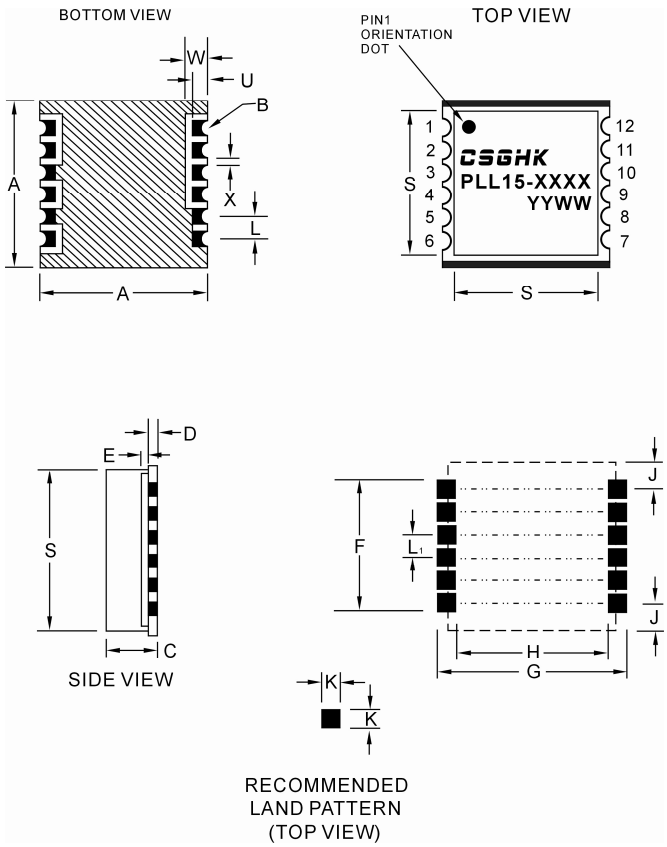
REVISIONS

NOTE，UNLESS OTHERWISE SPECIF IED：

1. THE METAL CASE IS GROUND
2. ALL HALF VIA CONTACTS ARE PLATED THRU FOROM THE PAD ON THE TOP SIDE TO THE PAD ON THE BOTTOM SIDE OF THE BOARD.
3. HATCHED AREAS GROUND AND ARE COVERED WINTH LPI SOLDER MASK OVER BARE COPPER. ALL CONTACT AREAS ARE PLATED. SIGNAL VIAS MAY BE LOCATED WITHIN GROUND PLANE.
4. SUBSTRATE MATERIAL：FR-4
5. XXXX PEPRFSENTS THE MODEL NUMBER.
6. YYWW IS THE DATA CODE.

PIN OUT FOR PLL	
PIN	APPLICATION
1	CLOCK
2	DATA
3	ENABLE
4	OSC IN
6	GROUND
7	VCC（VCO）
9	RF OUT
11	LOCK DETECT
12	VCC（CHIP）

ALL OTHER PINS ARE GROUND



SYMBOL	DIMENSION	
	MILLIMETERS	INCHES
A	15.24±0.25	0.60±0.010
B	R=0.50	R=0.020
C	3.50	0.138
D	0.99MAX	0.039MAX
E	0.51	0.020
F	11.68	0.460
G	17.07	0.672
H	14.02	0.552
J	2.54	0.100
K	1.50	0.059
L	2.00±0.05	0.080±0.002
L_1	2.00	0.080
S	14.60	0.575
U	1.28	0.050
W	1.78	0.070
X	0.51	0.020

	APPROVALS	DATA	CSGHK
DRAWN BY			
CHECKED BY			PLL-15 PACKAGE MECHANICAL PCB OUTLINE
PROCESS ENG			
QUALITY			
APPROVAL			