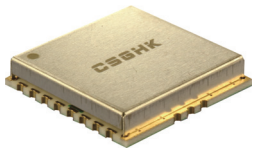
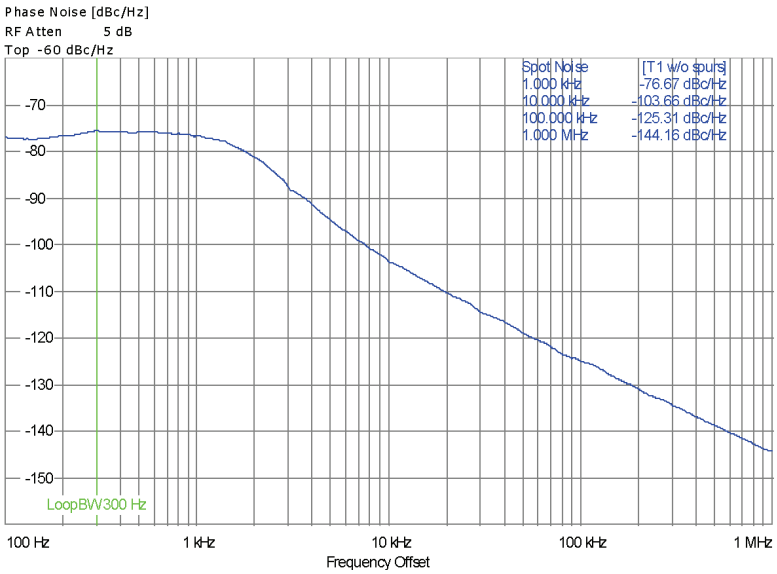
CSGHK

PHASE LOCKED LOOP

PLL15-2188M





FEATURES

- **Low Phase Noise**
- **Fast Settling Time**
- **Small Size,Surface Mount**
- **Integrated VCO, PLL IC, Loop Filter**

APPLICATLONS

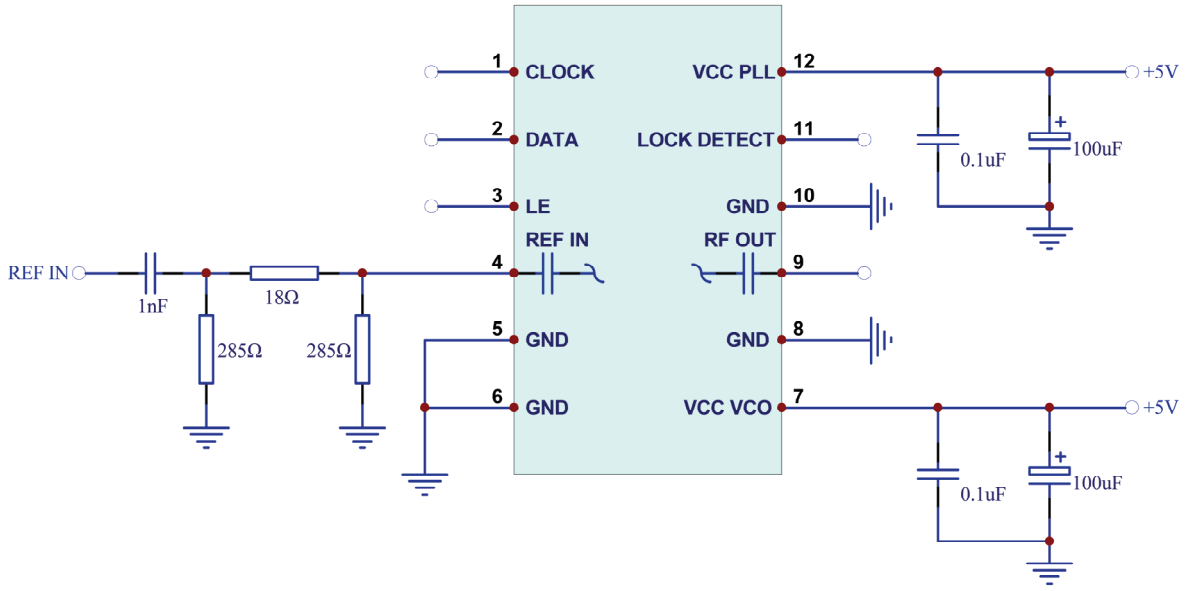
- **Commercial Wireless Applications**

Parameter	Min	Typ	Max	Units
Frequency Range -		2187.9		MHz
Step Size		100		KHz
Startup Lock Time		5.7		ms
Charge Pump Output Current		5.0		mA
Output Power -	0.0		4.0	dBm
Phase Noise:				
1 kHz		-76	-73	dBc/Hz
10 kHz		-103	-100	dBc/Hz
100 kHz		-125	-122	dBc/Hz
Spurious Product - 100KHz		-80	-70	dBc
Reference Feedthrough -		-80	-70	dBc
Harmonic Suppression -2nd		-20		dBc
Output Impedance -		50		Ω
OperatingTemperature Range	-40		+85	℃
Package Type	PLL-15(15.24X15.24X3.5mm)			
POWER SUPPLY REQUIREMENTS				
Supply Voltage	4.75	5	5.25	Vdc
Supply Current		32	35	mA
NOTES				
Reference Iput Fequency	5	13	104	MHz
Reference Iput Voltage	0.6		2.8	Vp-p
Phase Noise @ 1 kHz offset		-145		dBc/Hz

Shenzhen Sways Electronic Co., Ltd Tel：86-0755-83938305 Fax：86-0755-83512043 E-mail:csghk@csghk.com http://www.csghk.com

Recommended Application Circuit

Note: REF IN and RF OUT ports are internally AC coupled.



PLL Programming

Frequency Synthesizer PLL					ADF4113					3-wire serial 3.3V CMOS						
Register Map NOTE 1	F_Register	*Prescaler Value*		*Power-Dow2*	*Current Setting2*		*Current Setting 1*	*Timer Counter Control*	*Fastlock Mode*	*Fastlock Enable*	*CP Three-State*	*PD Polarity*	*Muxout Control*	*Power-Down 1*	*Counter Reset*	*Control Bits*
		10		0	111		111	0000	0	0	0	1	001	0	0	10
	R_Register @REF:13MHz PFD:100KHz	*Reserved*	*DLY*	*SYNC*	*Lock Detect Precision*	*Test ModeBits*	*Anti-Backlash Width*	*14-BIT Reference Counter, R*								*Control Bits*
		0	0	0	0	00	00	00000010000010								00
	N_Register @2187.9MHz	*Reserved*		*CP Gain*	*13-Bit B Counter*					*6-Bit A Counter*						*Control Bits*
		00		0	0001010101011					010111						01

Note 1: Registers Load Sequence: Initialization Register, F Register, R Register , N Register.

REVISIONS

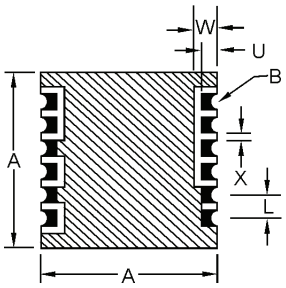
NOTE：UNLESS OTHERWISE SPECIF IED：

1. THE METAL CASE IS GROUND
2. ALL HALF VIA CONTACTS ARE PLATED THRU FOROM THE PAD ON THE TOP SIDE TO THE PAD ON THE BOTTOM SIDE OF THE BOARD.
3. HATCHED AREAS GROUND AND ARE COVERED WINTH LPI SOLDER MASK OVER BARE COPPER. ALL CONTACT AREAS ARE PLATED. SIGNAL VIAS MAY BE LOCATED WITHIN GROUND PLANE.
4. SUBSTRATE MATERIAL：FR-4
5. XXXX PEPRFSENTS THE MODEL NUMBER.
6. YYWW IS THE DATA CODE.

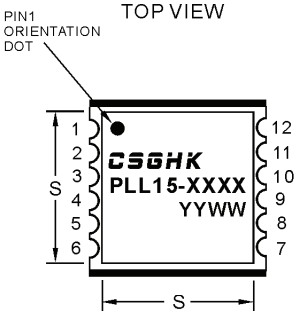
PIN OUT FOR PLL	
PIN	APPLICATION
1	CLOCK
2	DATA
3	ENABLE
4	REF IN
6	GROUND
7	VCC (VCO)
9	RF OUT
11	LOCK DETECT
12	VCC (CHIP)

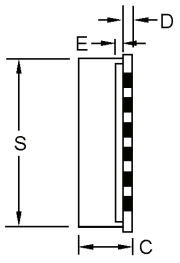
ALL OTHER PINS ARE GROUND

BOTTOM VIEW

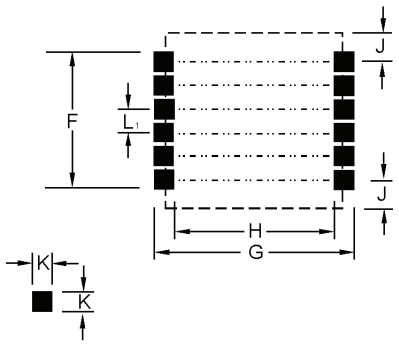


TOP VIEW





SIDE VIEW



RECOMMENDED
LAND PATTERN
(TOP VIEW)

SYMBOL	DIMENSION	
	MILLIMETERS	INCHES
A	15.24±0.25	0.60±0.010
B	R=0.50	R=0.020
C	3.50	0.138
D	0.99MAX	0.039MAX
E	0.51	0.020
F	11.68	0.460
G	17.07	0.672
H	14.02	0.552
J	2.54	0.100
K	1.50	0.059
L	2.00±0.05	0.080±0.002
L_1	2.00	0.080
S	14.60	0.575
U	1.28	0.050
W	1.78	0.070
X	0.51	0.020

	APPROVALS	DATA
DRAWN BY		
CHECKED BY		
PROCESS ENG		
QUALITY		
APPROVAL		

CSGHK

PLL-15 PACKAGE
MECHANICAL PCB OUTLINE

Shenzhen Sways Electronic Co., Ltd Tel：86-0755-83938305 Fax：86-0755-83512043 E-mail:csghk@csghk.com http://www.csghk.com