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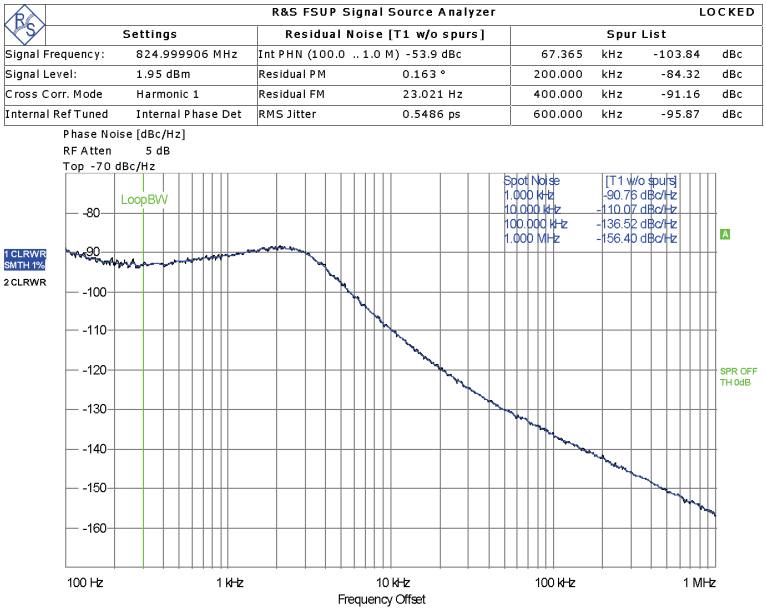
PHASE LOCKED LOOP

PLL20-825A



FEATURES

- Low Phase Noise
- Fast Settling Time
- Small Size,Surface Mount
- Integrated VCO, PLL IC, Loop Filter

APPLICATLONS

- Commercial Wireless Applications

Parameter	Min	Typ	Max	Units
Frequency Range -	800		850	MHz
Step Size		200		KHz
Startup Lock Time		3.0		ms
Charge Pump Output Current		4.2		mA
Output Power -	0.0		4.0	dBm
Phase Noise:				
1 kHz		-89	-86	dBc/Hz
10 kHz		-110	-107	dBc/Hz
100 kHz		-137	-134	dBc/Hz
Spurious Product - 200KHz		-80	-70	dBc
Reference Feedthrough -		-80	-70	dBc
Harmonic Suppression -2nd		-25		dBc
Output Impedance -		50		Ω
OperatingTemperature Range	-40		+85	℃
Package Type	PLL-20(20.3X14.8X3.5mm)			
POWE SUPPLY REQUIREMENTS				
Supply Voltage	4.85	5	5.15	Vdc
Supply Current		26	29	mA
NOTES				
Reference Iput Fequency	5	13	104	MHz
Reference Iput Voltage	0.4		3.0	Vp-p
Frequency Synthesizer IC	ADF4113			

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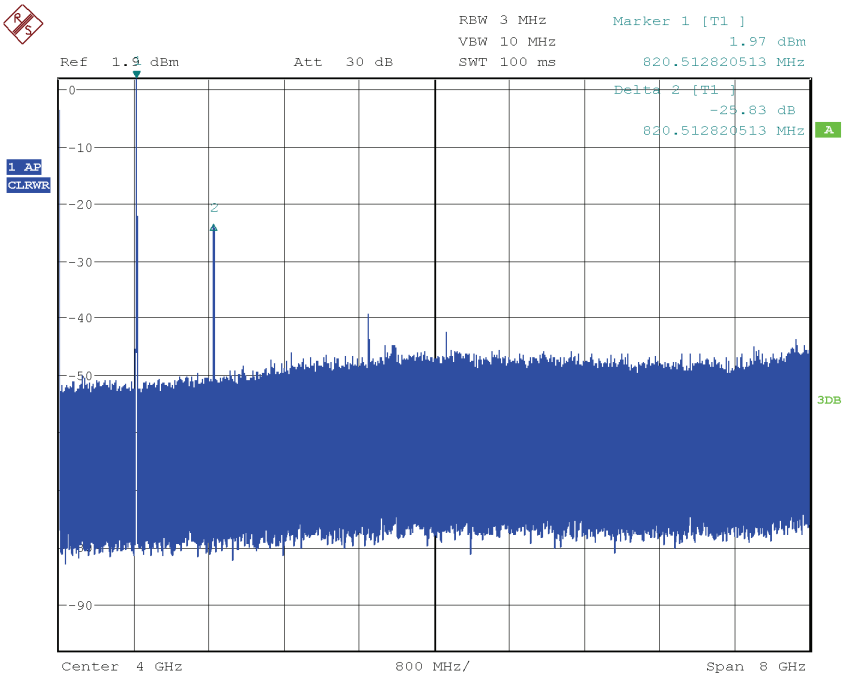

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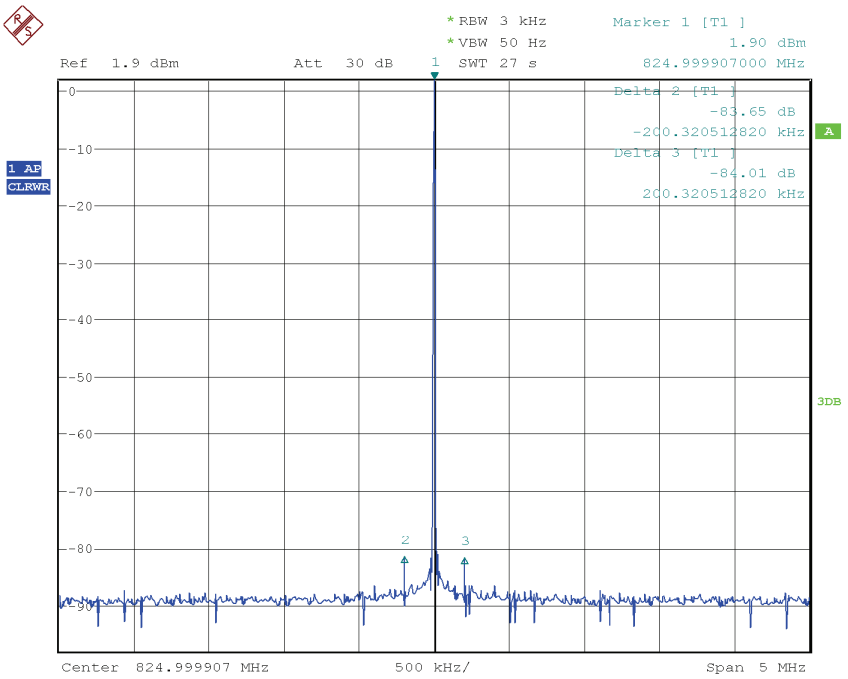

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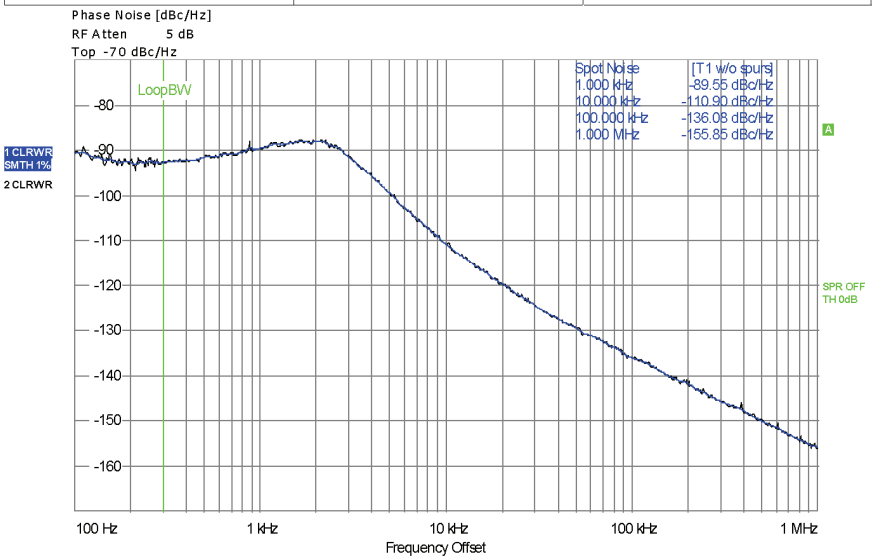
R&S FSUP Signal Source Analyzer — LOCKED

Settings		Residual Noise [T1 w/o spurs]		Spur List			
Signal Frequency:	800.999915 MHz	Int PHN (100.0 .. 1.0 M)	-53.8 dBc	67.368	kHz	-102.83	dBc
Signal Level:	1.54 dBm	Residual PM	0.165 °	200.000	kHz	-94.48	dBc
Cross Corr. Mode	Harmonic 1	Residual FM	23.645 Hz	400.000	kHz	-100.17	dBc
Internal Ref Tuned	Internal Phase Det	RMS Jitter	0.5729 ps	599.999	kHz	-103.48	dBc



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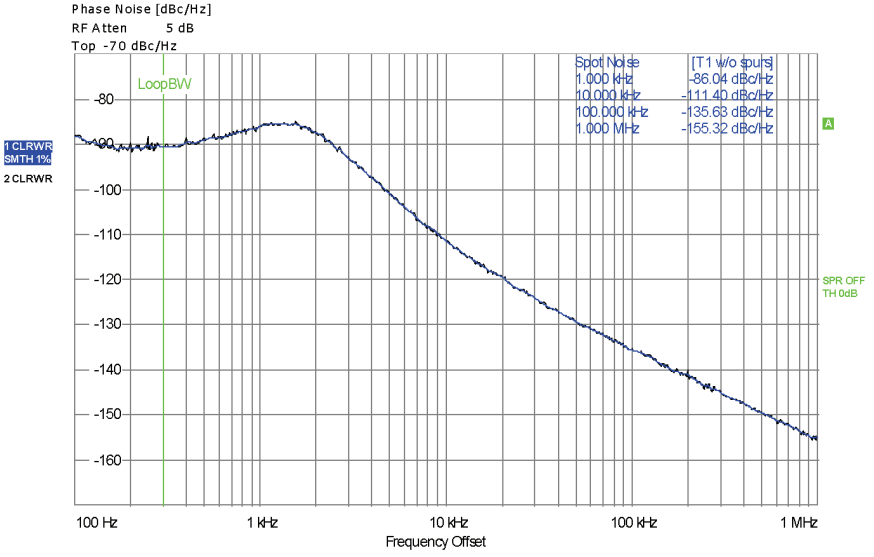
R&S FSUP Signal Source Analyzer — LOCKED

Settings		Residual Noise [T1 w/o spurs]		Spur List			
Signal Frequency:	845.999908 MHz	Int PHN (100.0 .. 1.0 M)	-52.7 dBc	149.840	Hz	-84.38	dBc
Signal Level:	2.02 dBm	Residual PM	0.189 °	239.990	Hz	-82.19	dBc
Cross Corr. Mode	Harmonic 1	Residual FM	24.352 Hz	249.657	Hz	-82.80	dBc
Internal Ref Tuned	Internal Phase Det	RMS Jitter	0.6192 ps	877.965	Hz	-77.12	dBc



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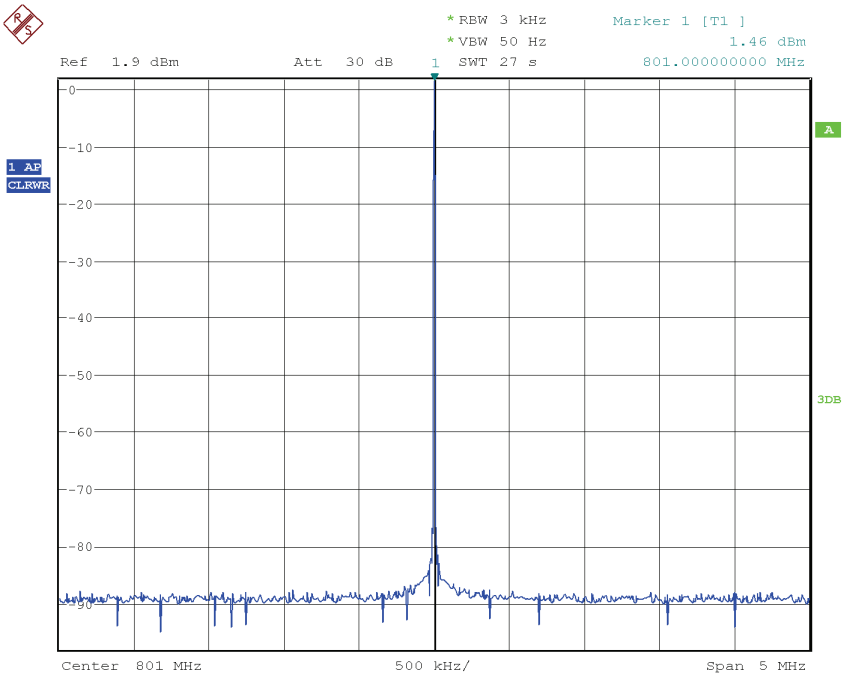

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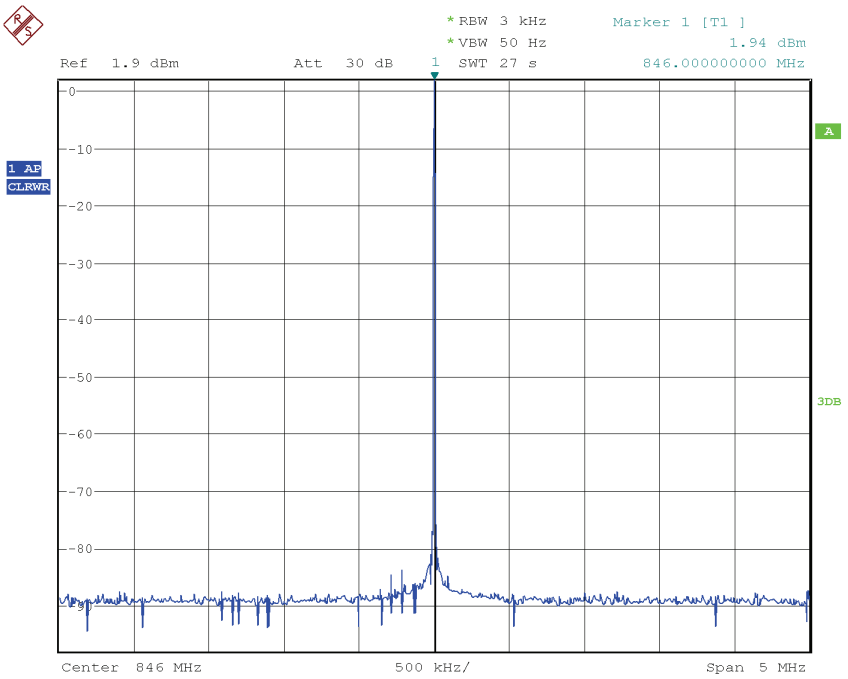

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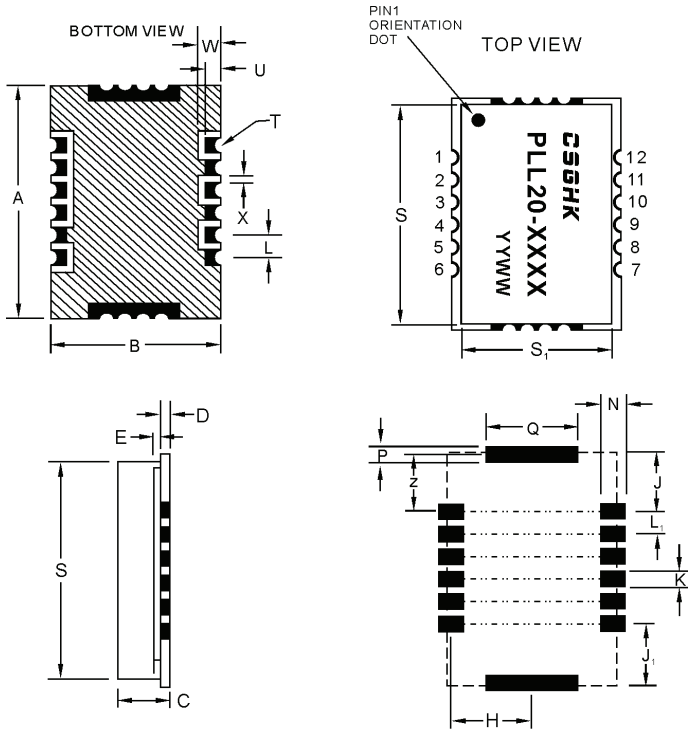
REVISIONS

NOTE：UNLESS OTHERWISE SPECIF IED:

1. THE METAL CASE IS GROUND
2. ALL HALF VIA CONTACTS ARE PLATED THRU FOROM THE PAD ON THE TOP SIDE TO THE PAD ON THE BOTTOM SIDE OF THE BOARD.
3. HATCHED AREAS GROUND AND ARE COVERED WINTH LPI SOLDER MASK OVER BARE COPPER. ALL CONTACT AREAS ARE PLATED. SIGNAL VIAS MAY BE LOCATED WITHIN GROUND PLANE.
4. SUBSTRATE MATERIAL：FR-4
5. XXXX PEPRFSENTS THE MODEL NUMBER.
6. YYWW IS THE DATA CODE.

PIN OUT FOR PLL	
PIN	APPLICATION
1	VCC (CHIP)
3	OSC IN
5	VCC (VCO)
7	RF OUT
9	LOCK DETECT
10	CLOCK
11	DATA
12	ENABLE

ALL OTHER PINS ARE GROUND



SYMBOL	DIMENSION	
	MILLIMETERS	INCHES
A	20.3±0.25	0.800±0.010
B	14.8±0.25	0.582±0.010
C	3.50	0.138
D	0.99MAX	0.039MAX
E	0.51	0.020
H	6.91	0.272
J	5.16	0.203
J_1	5.13	0.202
K	1.50	0.059
L	2.00±0.05	0.080±0.002
L_1	2.00	0.080
N	1.98	0.078±0.003
P	1.52	0.060±0.003
Q	7.40	0.291±0.003
S	19.56	0.770
S_1	14.02	0.552
T	R=0.50	R=0.020
U	1.47	0.058
W	1.78	0.070
X	0.51	0.020
Z	4.90	0.193

	APPROVALS	DATA
DRAWN BY		
CHECKED BY		
PROCESS ENG		
QUALITY		

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PLL-20 PACKAGE
MECHANICAL PCB OUTLINE