

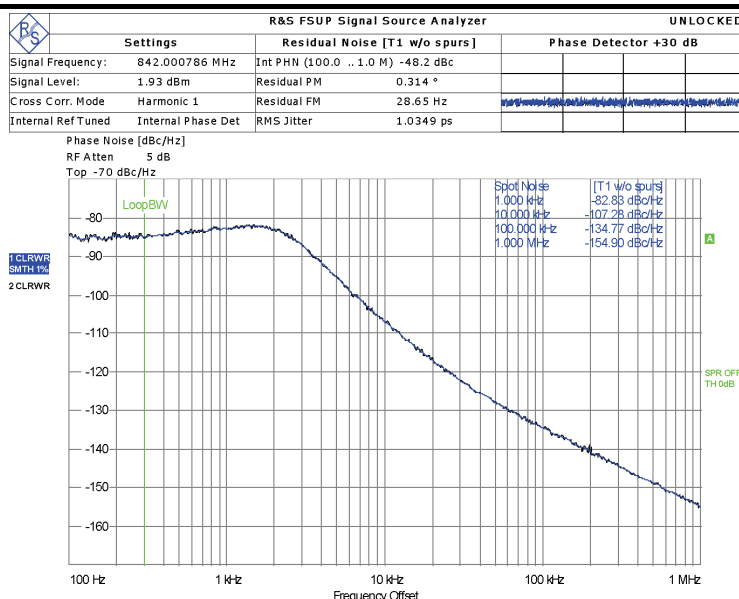


FEATURES

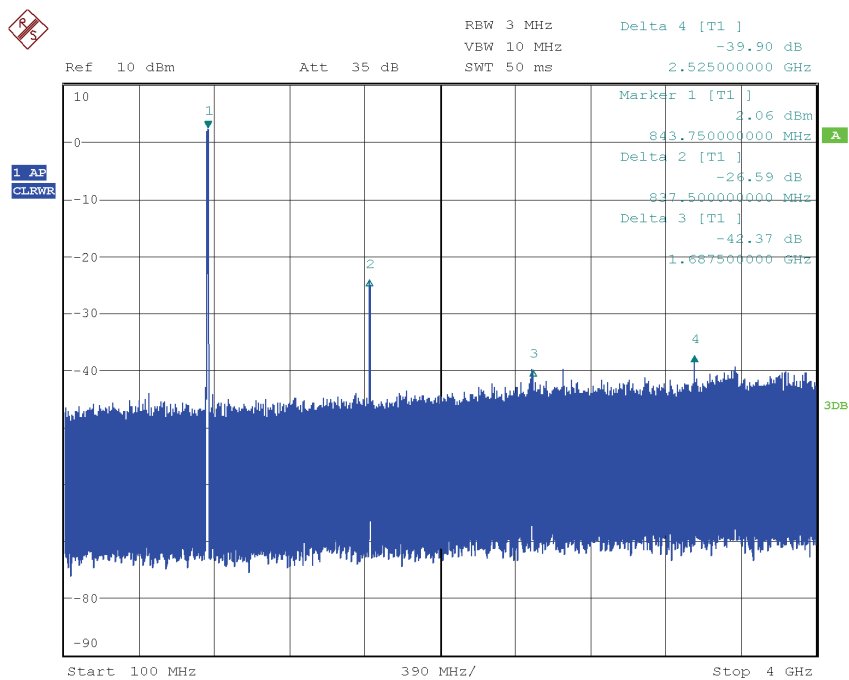
- ◆ Low Phase Noise
- ◆ Fast Settling Time
- ◆ Small Size, Surface Mount
- ◆ Integrated VCO, PLL IC, Loop Filter

APPLICATIONS

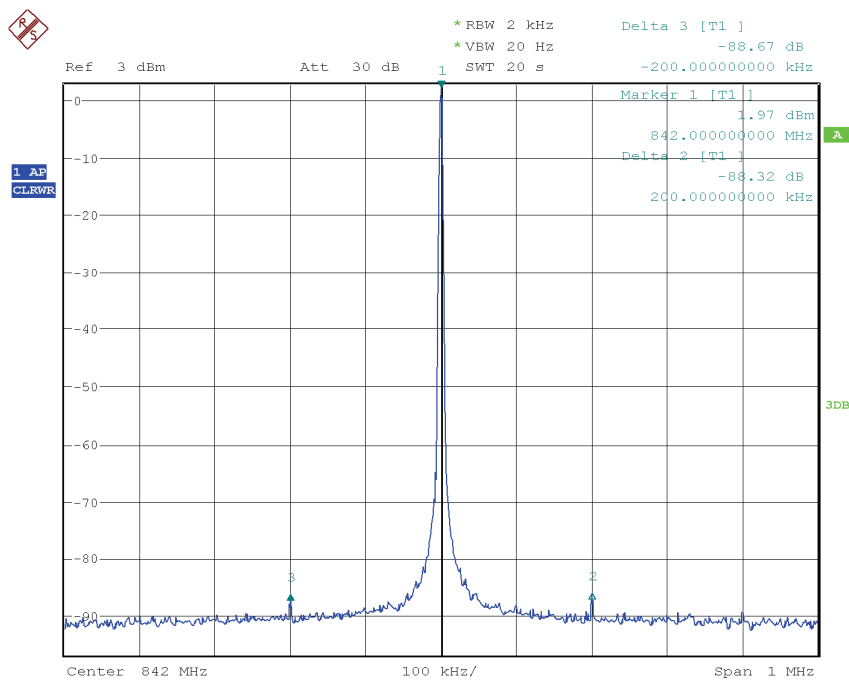
- ◆ Commercial Wireless Applications



Parameter	Min	Typ	Max	Units
Frequency Range -	830		854	MHz
Step Size		200		KHz
Startup Lock Time		3.6		ms
Charge Pump Output Current		1.0		mA
Output Power -	0.0		4.0	dBm
Phase Noise:				
1 kHz		-82	-80	dBc/Hz
10 kHz		-106	-104	dBc/Hz
100 kHz		-134	-132	dBc/Hz
Spurious Product - 200KHz		-80	-70	dBc
Reference Feedthrough -		-80	-70	dBc
Harmonic Suppression -2nd		-25		dBc
Output Impedance -		50		Ω
OperatingTemperature Range	-40		+85	℃
Package Type	PLL-20(20.3X14.8X3.5mm)			
POWE SUPPLY REQUIREMENTS				
Supply Voltage	4.85	5	5.15	Vdc
Supply Current		27	30	mA
NOTES				
Reference Iput Frequency		10		MHz
Reference Iput Voltage	0.4		3.0	Vp-p
Frequency Synthesizer IC	LMX2326			



Date: 16.APR.2009 11:39:12



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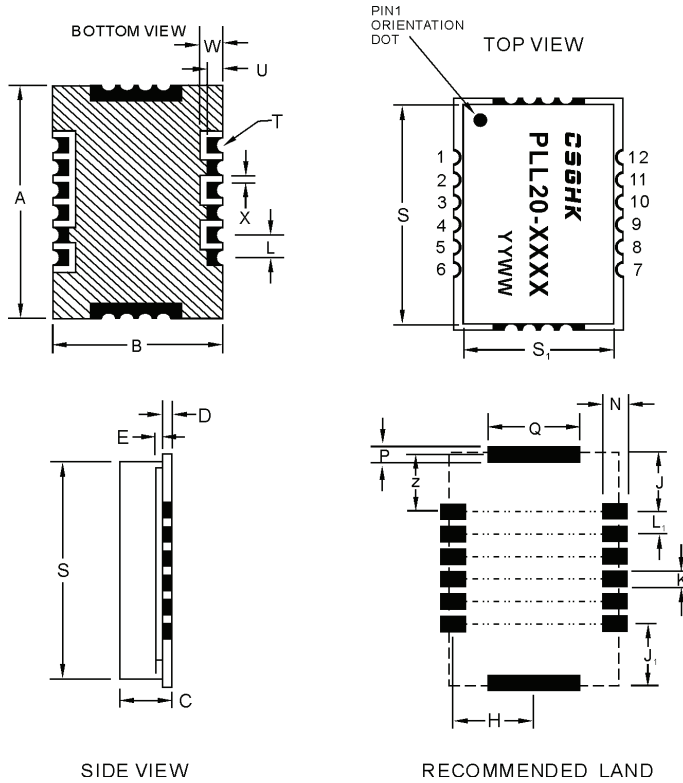
REVISIONS

NOTE. UNLESS OTHERWISE SPECIFIED:

1. THE METAL CASE IS GROUND
2. ALL HALF VIA CONTACTS ARE PLATED THRU FROM THE PAD ON THE TOP SIDE TO THE PAD ON THE BOTTOM SIDE OF THE BOARD.
3. HATCHED AREAS GROUND AND ARE COVERED WITH LPI SOLDER MASK OVER BARE COPPER. ALL CONTACT AREAS ARE PLATED. SIGNAL VIAS MAY BE LOCATED WITHIN GROUND PLANE.
4. SUBSTRATE MATERIAL: FR-4
5. XXXX REPRESENTS THE MODEL NUMBER.
6. YYWW IS THE DATA CODE.

PIN OUT FOR PLL	
PIN	APPLICATION
1	VCC (CHIP)
3	OSC IN
5	VCC (VCO)
7	RF OUT
9	LOCK DETECT
10	CLOCK
11	DATA
12	ENABLE

ALL OTHER PINS ARE GROUND



SYMBOL	DIMENSION	
	MILLIMETERS	INCHES
A	20.3±0.25	0.800±0.010
B	14.8±0.25	0.582±0.010
C	3.50	0.138
D	0.99MAX	0.039MAX
E	0.51	0.020
H	6.91	0.272
J	5.16	0.203
J ₁	5.13	0.202
K	1.50	0.059
L	2.00±0.05	0.080±0.002
L ₁	2.00	0.080
N	1.98	0.078±0.003
P	1.52	0.060±0.003
Q	7.40	0.291±0.003
S	19.56	0.770
S ₁	14.02	0.552
T	R=0.50	R=0.020
U	1.47	0.058
W	1.78	0.070
X	0.51	0.020
Z	4.90	0.193

	APPROVALS	DATA	 PLL-20 PACKAGE MECHANICAL PCB OUTLINE
DRAWN BY			
CHECKED BY			
PROCESS ENG			
QUALITY			