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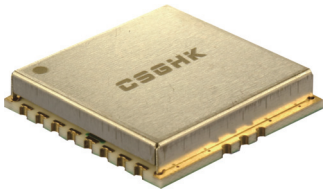
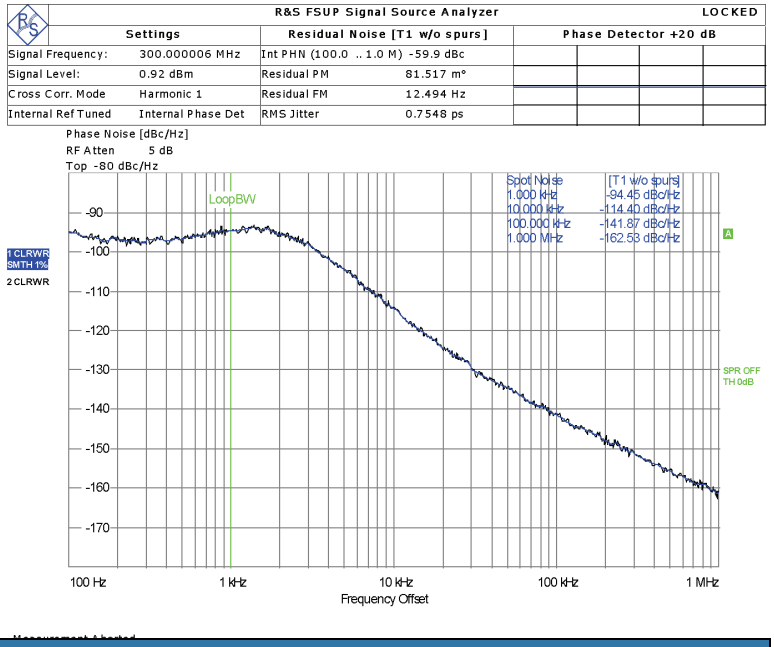
PHASE LOCKED LOOP

PLL25A-300M





FEATURES

- Low Phase Noise
- Fast Settling Time
- Small Size,Surface Mount
- Integrated VCO, PLL IC, Loop Filter

APPLICATLONS

- Commercial Wireless Applications

Parameter	Min	Typ	Max	Units
Frequency Range -	290		310	MHz
Step Size		200		KHz
Startup Lock Time		2.9		ms
Charge Pump Output Current		5.0		mA
Output Power -	-2.0		2.0	dBm
Phase Noise:				
1 kHz		-93	-90	dBc/Hz
10 kHz		-113	-110	dBc/Hz
100 kHz		-140	-137	dBc/Hz
Spurious Product - 200KHz		-80	-70	dBc
Reference Feedthrough -		-80	-70	dBc
Harmonic Suppression -2nd		-20		dBc
Output Impedance -		50		Ω
OperatingTemperature Range	-40		+85	℃
Package Type	PLL-25A(19.05X19.05X3.5mm)			
POWER SUPPLY REQUIREMENTS				
Supply Voltage	4.75	5	5.25	Vdc
Supply Current		19	21	mA
NOTES				
Reference Iput Fequency	5	13	104	MHz
Reference Iput Voltage	0.4		3.0	Vp-p
Frequency Synthesizer IC	ADF4113			

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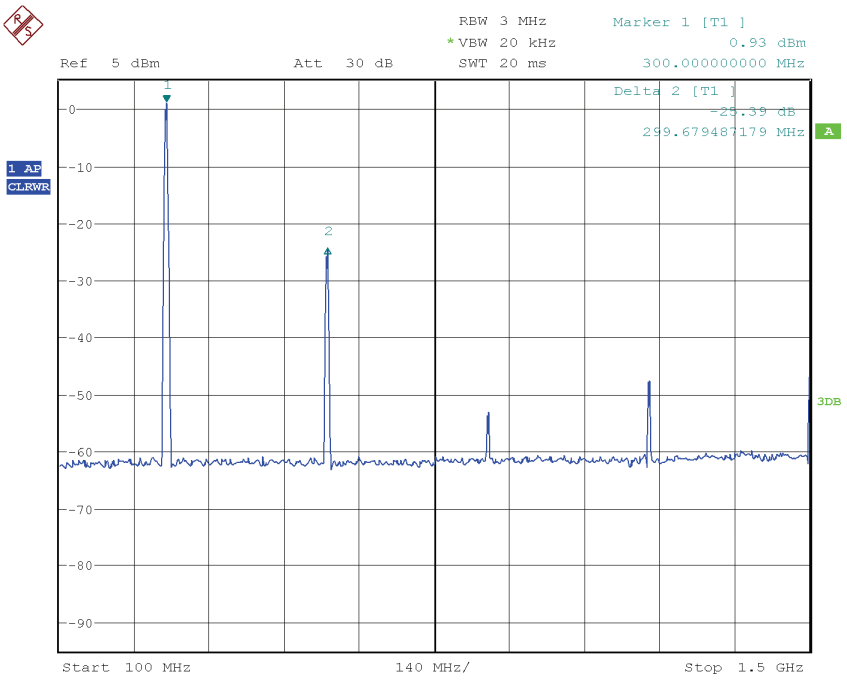

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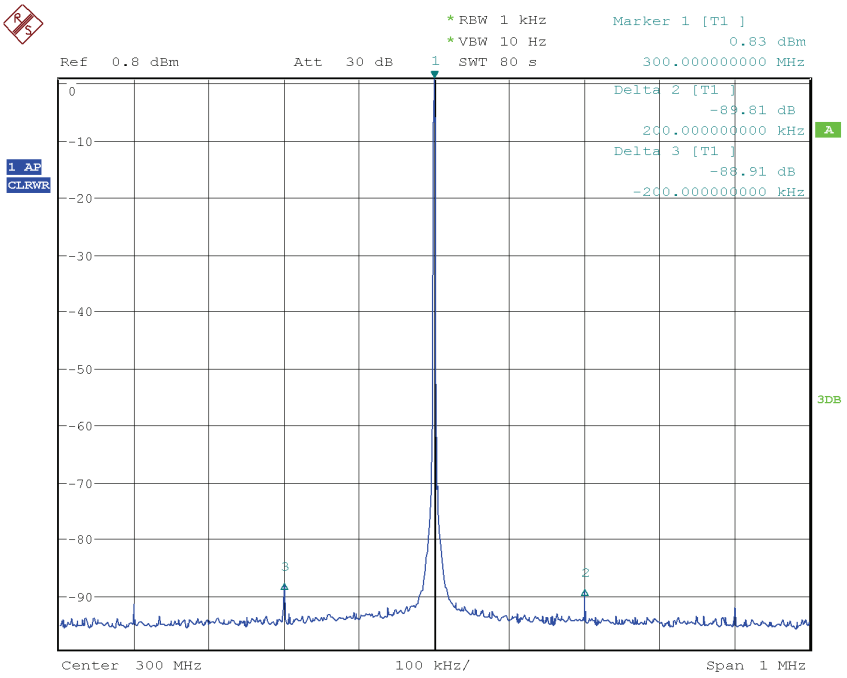

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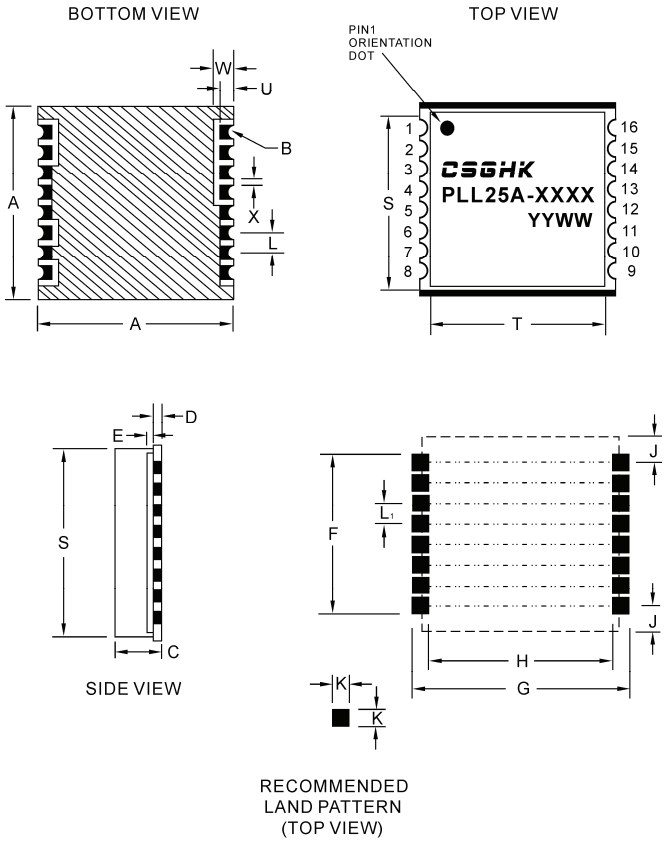
REVISIONS

NOTE：UNLESS OTHERWISE SPECIF IED：

1. THE METAL CASE IS GROUND
2. ALL HALF VIA CONTACTS ARE PLATED THRU FOROM THE PAD ON THE TOP SIDE TO THE PAD ON THE BOTTOM SIDE OF THE BOARD.
3. HATCHED AREAS GROUND AND ARE COVERED WINTH LPI SOLDER MASK OVER BARE COPPER. ALL CONTACT AREAS ARE PLATED. SIGNAL VIAS MAY BE LOCATED WITHIN GROUND PLANE.
4. SUBSTRATE MATERIAL：FR-4
5. XXXX PEPRFSENTS THE MODEL NUMBER.
6. YYWW IS THE DATA CODE.

PIN OUT FOR PLL			
PIN	APPLICATION	PIN	APPLICATION
1	OSC IN	9	VCC (VCO)
2	ENABLE	11	RF OUT
3	DATA	15	VCC (CHIP)
4	CLOCK	16	LOCK DETECT

ALL OTHER PINS ARE GROUND



SYMBOL	DIMENSION	
	MILLIMETERS	INCHES
A	19.05±0.25	0.75±0.010
B	R=0.50	R=0.020
C	3.50	0.138
D	0.99MAX	0.039MAX
E	0.60	0.023
F	15.75	0.620
G	20.57	0.810
H	17.53	0.690
J	2.41	0.095
K	1.50	0.059
L	2.00±0.05	0.080±0.002
L_1	2.00	0.080
S	18.03	0.710
T	18.19	0.716
U	1.28	0.050
W	1.78	0.070
X	0.51	0.020

	APPROVALS	DATA
DRAWN BY		
CHECKED BY		
PROCESS ENG		
QUALITY		
APPROVAL		

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PLL-25A PACKAGE
MECHANICAL PCB OUTLINE