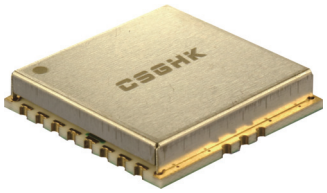
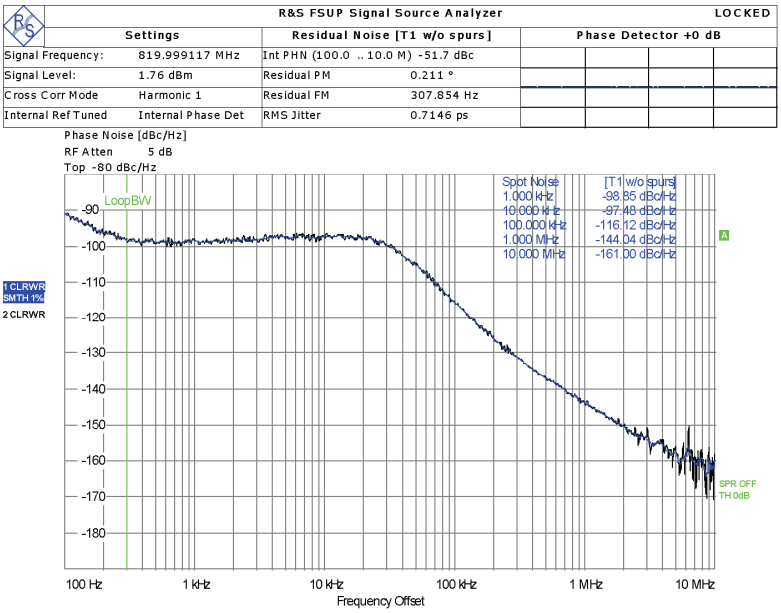
CSGHK

PHASE LOCKED LOOP

PLL25A-820M





FEATURES

- Low Phase Noise
- Fast Settling Time
- Small Size,Surface Mount
- Integrated VCO, PLL IC, Loop Filter

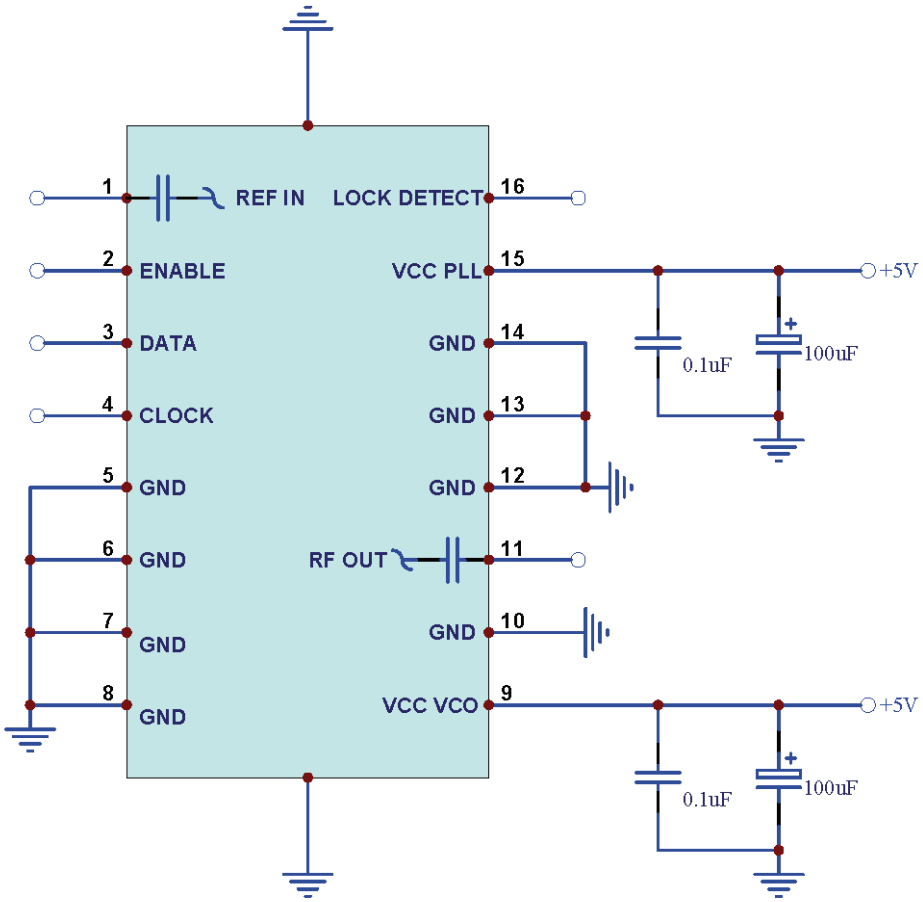
APPLICATLONS

- Commercial Wireless Applications

Parameter	Min	Typ	Max	Units
Frequency Range -	720		920	MHz
Step Size		1000		KHz
Startup Lock Time		301		us
Charge Pump Output Current		5.0		mA
Output Power -	0.0		4.0	dBm
Phase Noise:				
1 kHz		-98	-95	dBc/Hz
10 kHz		-97	-94	dBc/Hz
100 kHz		-116	-113	dBc/Hz
Spurious Product - 1000KHz		-80	-70	dBc
Reference Feedthrough -		-80	-70	dBc
Harmonic Suppression -2nd		-20		dBc
Output Impedance -		50		Ω
OperatingTemperature Range	-40		+85	℃
Package Type	PLL-25A(19.05X19.05X3.5mm)			
POWER SUPPLY REQUIREMENTS				
Supply Voltage	4.75	5	5.25	Vdc
Supply Current		40	43	mA
NOTES				
Reference Iput Fequency	5	13	104	MHz
Reference Iput Voltage	0.4		3.0	Vp-p
Phase Noise @ 1 kHz offset		-145		dBc/Hz

Recommended Application Circuit

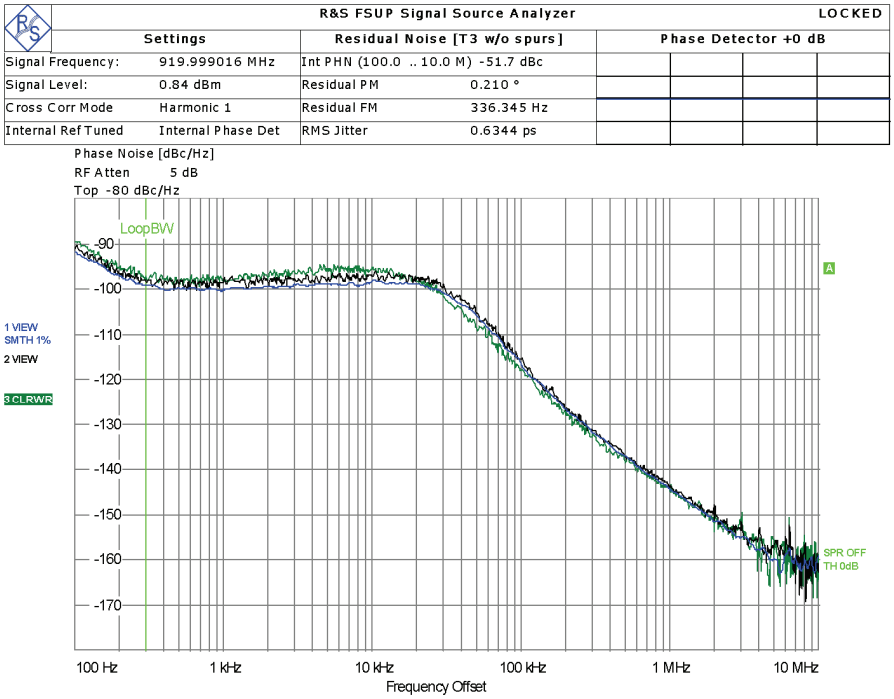
Note: REF IN and RF OUT ports are internally AC coupled.

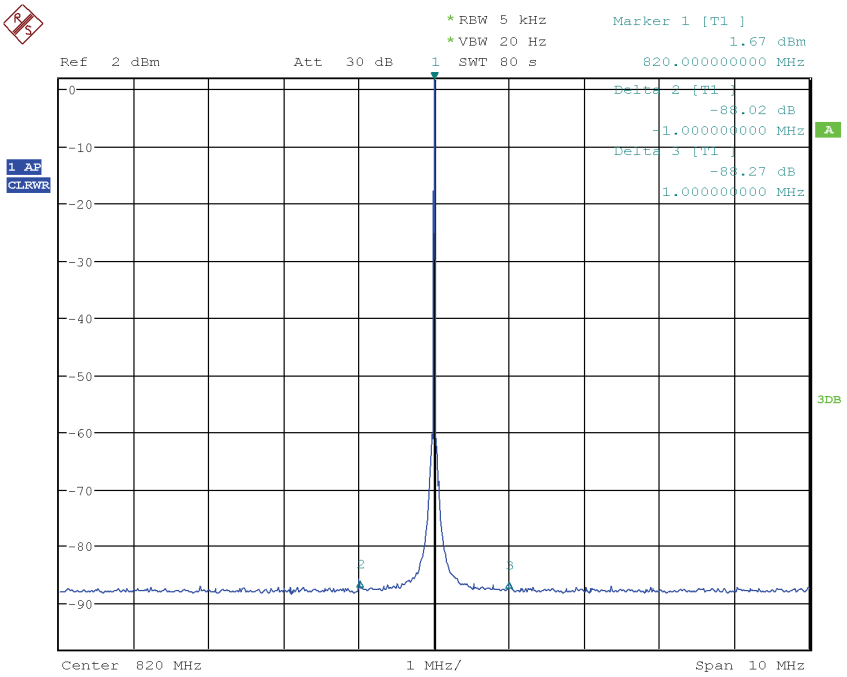


PLL Programming

Frequency Synthesizer PLL					ADF4113					3-wire serial 3.3V CMOS						
Register Map NOTE 1	F_Register	*Prescaler Value*		*Power-Dow2*	*Current Setting2*		*Current Setting 1*	*Timer Counter Control*	*Fastlock Mode*	*Fastlock Enable*	*CP Three-State*	*PD Polarity*	*Muxout Control*	*Power-Down 1*	*Counter Reset*	*Control Bits*
		01		0	111		111	0000	0	0	0	1	001	0	0	11
	R_Register @REF:13MHz PFD:1000KHz	*Reserved*	*DLY*	*SYNC*	*Lock Detect Precision*	*Test ModeBits*	*Anti-Backlash Width*	*14-BIT Reference Counter, R*								*Control Bits*
		0	0	0	0	00	00	00000000001101								00
	N_Register @820MHz	*Reserved*		*CP Gain*	*13-Bit B Counter*					*6-Bit A Counter*						*Control Bits*
		00		0	0000000110011					000100						01

Note 1: Registers Load Sequence: Initialization Register, F Register, R Register , N Register.





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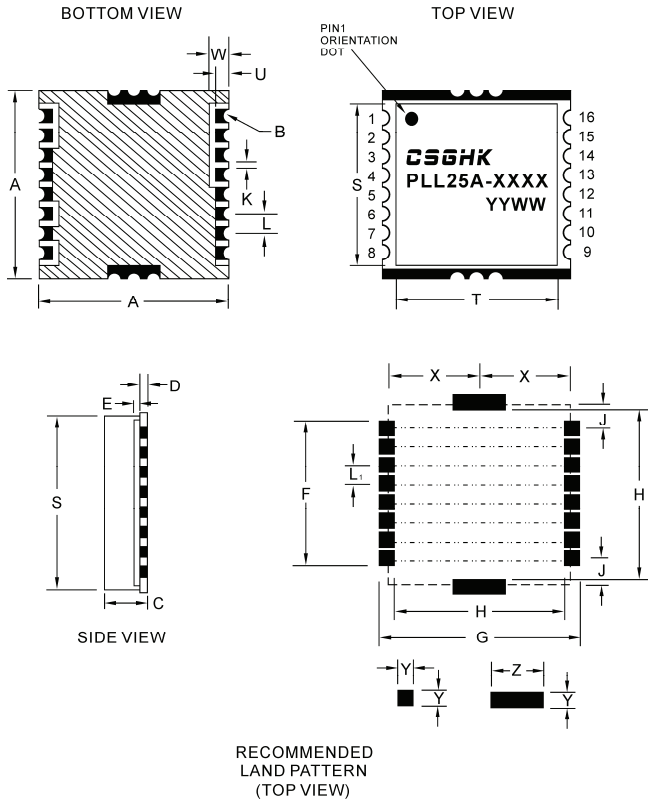
REVISIONS

NOTE：UNLESS OTHERWISE SPECIF IED：

1. THE METAL CASE IS GROUND
2. ALL HALF VIA CONTACTS ARE PLATED THRU FOROM THE PAD ON THE TOP SIDE TO THE PAD ON THE BOTTOM SIDE OF THE BOARD.
3. HATCHED AREAS GROUND AND ARE COVERED WINTH LPI SOLDER MASK OVER BARE COPPER. ALL CONTACT AREAS ARE PLATED. SIGNAL VIAS MAY BE LOCATED WITHIN GROUND PLANE.
4. SUBSTRATE MATERIAL：FR-4
5. XXXX PEPRFSENTS THE MODEL NUMBER.
6. YYWW IS THE DATA CODE.

PIN OUT FOR PLL			
PIN	APPLICATION	PIN	APPLICATION
1	REF IN	9	VCC (VCO)
2	ENABLE	11	RF OUT
3	DATA	15	VCC (CHIP)
4	CLOCK	16	LOCK DETECT

ALL OTHER PINS ARE GROUND



SYMBOL	DIMENSION	
	MILLIMETERS	INCHES
A	19.05±0.25	0.75±0.010
B	R=0.425	R=0.017
C	3.50	0.138
D	0.99MAX	0.039MAX
E	0.60	0.023
F	15.75	0.620
G	20.57	0.810
H	17.53	0.690
J	2.41	0.095
K	0.51	0.020
L	2.00±0.05	0.080±0.002
L_1	2.00	0.080
S	18.03	0.710
T	18.19	0.716
U	1.28	0.050
W	1.78	0.070
X	9.5	0.374
Y	1.50	0.059
Z	5.5	0.217

	APPROVALS	DATA
DRAWN BY		
CHECKED BY		
PROCESS ENG		
QUALITY		
APPROVAL		

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PLL-25A PACKAGE
MECHANICAL PCB OUTLINE