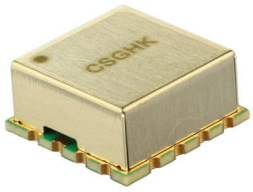
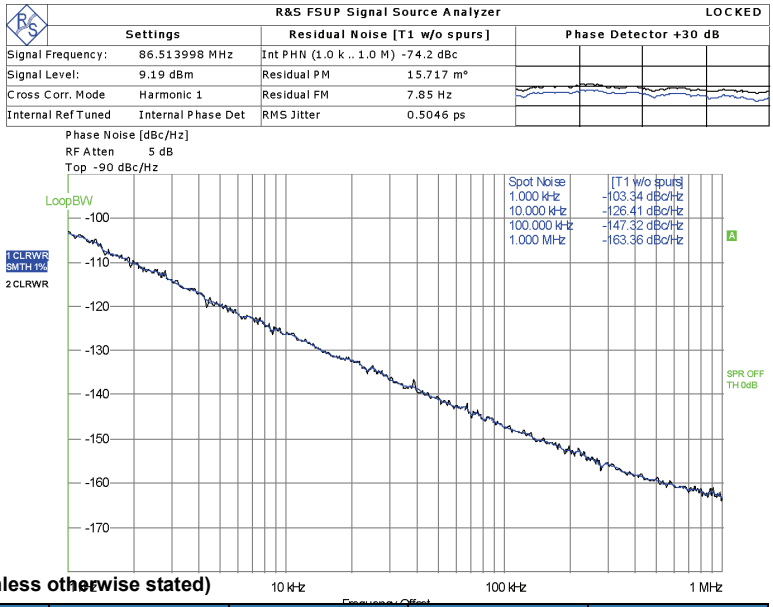
CSGHK

SURFACE MOUNT MODEL
VOLTAGE CONTROLLED OSCILLATOR

Frequency **72-102MHz** **VLN102A**





FEATURES
▶ **Miniature Size**
▶ **Surface Mount Package**
▶ **Low Phase Noise Performance**
▶ **Electrically Shielded**
▶ **Highly Linear Tuning**

Electrical Specifications,T_A = +25℃,V_{CC} = +5.0V(unless otherwise stated)

Parameter	Test Conditions	Min	Typ	Max	Units
Frequency Rangs		72		102	MHz
Tuning Voltage (V)		2.5		9.5	V
RF Output Power	72-102MHz	7.0		11.0	dBm
Supply Voltage (Vcc)		4.75	5	5.25	V
Supply Current (Icc)			23	26	mA
Phase Noise：					
	@10kHz Offset:		-125	-122	dBc/Hz
	@100kHz Offset:		-146	-143	dBc/Hz
Average Tuning Sensitivity	72-102MHz		4.6		MHz/V
Harmonic Outputs			-20		dBc
OperatingTemperature Range		-55		+85	℃
Tune Input Capacitance			1000		PF
Output Impedance -			50		Ω
Package Type	SK605G(12.7X12.7X5.8mm)				

Comments

X Indicates parameter to be tested 100% in production

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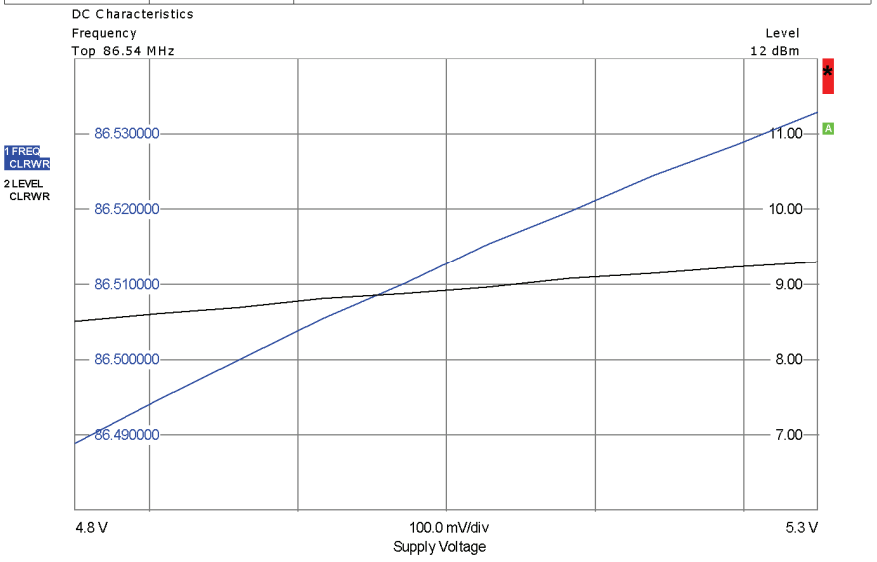
V TUNE	TUNING SENS. (MHz/V)	FREQUENCY(MHz) -55℃	+25℃	+85℃	POWER OUTPUT(dBm) -55℃	+25℃	+85℃	HARMONIC(dBc) 2^n -55℃	+25℃	+85℃
2.5	5.6	71.19	70.23	69.55	6.9	7.6	6.8	-14.6	-17.0	-22.1
3.5	5.5	76.81	75.76	75.06	7.2	7.8	6.8	-17.6	-19.9	-24.4
4.5	5.5	82.34	81.26	80.56	7.6	8.0	6.9	-21.3	-23.6	-27.5
5.5	5.4	87.61	86.66	85.85	8.4	8.5	7.1	-24.7	-27.6	-31.1
6.5	4.8	92.49	91.62	90.75	8.9	8.6	7.1	-27.5	-31.4	-35.6
7.5	4.3	96.93	96.04	95.13	8.7	8.4	6.9	-29.9	-35.2	-41.7
8.5	3.8	100.94	99.97	99.05	8.3	8.0	6.6	-31.0	-36.4	-54.5
9.5	3.4	104.45	103.45	102.48	7.7	7.5	6.3	-31.0	-35.8	-49.7

R&S FSUP Signal Source Analyzer

Settings			Results		
Supply	Voltage		Frequency		Level	
Vmin	4.75	V	86.489	MHz	8.50	dBm
Vcurrent	5.00	V	86.512	MHz	8.92	dBm
Vmax	5.25	V	86.533	MHz	9.29	dBm



Measurement Aborted

Date: 5.SEP.2009 15:08:44

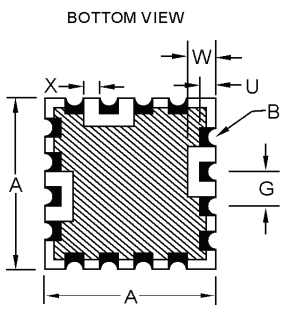
REVISIONS

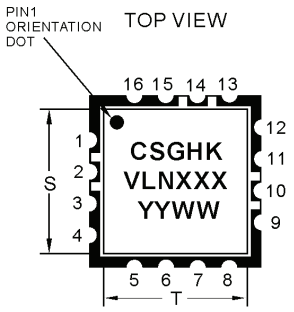
NOTE，UNLESS OTHERWISE SPECIF IED：

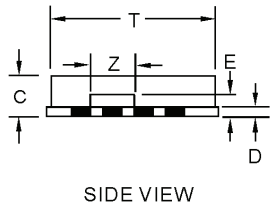
1. THE METAL CASE IS GROUND
2. ALL HALF VIA CONTACTS ARE PLATED THRU FOROM THE PAD ON THE TOP SIDE TO THE PAD ON THE BOTTOM SIDE OF THE BOARD.
3. HATCHED AREAS GROUND AND ARE COVERED WINTH LPI SOLDER MASK OVER BARE COPPER. ALL CONTACT AREAS ARE PLATED. SIGNAL VIAS MAY BE LOCATED WITHIN GROUND PLANE.
4. SUBSTRATE MATERIAL：FR-4
5. XXXX PEPRFSENTS THE MODEL NUMBER.
6. YYWW IS THE DATA CODE.

PIN OUT FOR PLL	
PIN	APPLICATION
2	VT
10	RF OUT
14	VCC

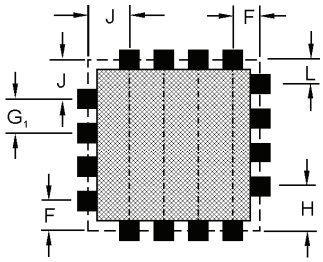
ALL OTHER PINS ARE GROUND







SIDE VIEW



RECOMMENDED
LAND PATTERN
(TOP VIEW)

SYMBOL	DIMENSION	
	MILLIMETERS	INCHES
A	12.7±0.25	0.50±0.010
B	R=0.50	R=0.019
C	5.80	0.228
D	0.99MAX	0.039MAX
E	1.75MAX	0.069MAX
F	2.16	0.085
G	2.54±0.08	0.100±0.003
G_1	2.54	0.100
H	3.07	0.121
J	2.92	0.115
K	1.52	0.060
L	2.00	0.079
S	11.68	0.460
T	11.81	0.465
U	1.10	0.043
W	1.78	0.188
X	1.02	0.040
Z	3.49	0.137

	APPROVALS	DATA
DRAWN BY		
CHECKED BY		
PROCESS ENG		
QUALITY		

CSGHK

SK605G PACKAGE
MECHANICAL PCB OUTLINE

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